CLAIMS

What is claimed is:

1. An apparatus comprising:

at least one stage having a first input terminal that receives a first test voltage, a second input terminal that receives a first reference voltage, a third input terminal that receives a second test voltage, and a fourth input terminal that receives a second reference voltage, said at least one stage having a first output terminal upon which is produced a first test signal that is proportional to said first test voltage, a second output terminal upon which is produced a first reference signal that is proportional to said first reference voltage, a third output terminal upon which is produced a second test signal that is proportional to said second test voltage, and a fourth output terminal upon which is produced a second reference signal that is proportional to said second reference voltage;

a switching circuit coupled to said at least one stage, said switching circuit having a first output terminal that is switchably coupled to said first output terminal and one of said third output terminal and said fourth output terminal of said at least one stage, said switching circuit having a second output terminal that is switchably coupled to said first output terminal and one of said third output terminal and said fourth output terminal of said at least one stage; and

a comparator circuit having a first input terminal coupled to said first output terminal of said switching circuit and a second input terminal coupled to said second output terminal of said switching circuit.

2. The apparatus of Claim 1, wherein said at least one stage is at least one transconductance stage, and wherein said first test signal is a first test current and said second test signal is a second test current, and wherein said first reference signal is a first reference current and said second reference signal is a second reference current.

3. The apparatus of Claim 1, wherein said at least one stage is a differential amplifier and wherein said first test signal, said second test signal, said first reference signal, and said second reference signal are voltage signals.

and wherein said first test signal, and said second test signal are a first test voltage and a second test voltage, and wherein said first reference signal and said second reference signal are a first reference voltage and a second reference voltage.

4. The apparatus of Claim 2, wherein said at least one transconductance stage comprises:

a first transconductance stage having said first input terminal, said second input terminal, said first output terminal and said second output terminal; and

a second transconductance stage having said third input terminal, said fourth input terminal, said third output terminal and said fourth output terminal.

5. The apparatus of Claim 2, wherein said switching circuit comprises:

a first transistor coupled between said third output terminal of said at least one transconductance circuit and said first output terminal of said switching circuit;

a second transistor coupled between said third output terminal of said at least one transconductance circuit and said second output terminal of said switching circuit;

a third transistor coupled between said fourth output terminal of said at least one transconductance circuit and said first output terminal of said switching circuit; and

a fourth transistor coupled between said third output terminal of said at least one transconductance circuit and said second output terminal of said switching circuit;

wherein the bases of said first transistor and said fourth transistor are coupled together and the bases of said second transistor and said third transistor are coupled together.

6. The apparatus of Claim 5, wherein said switching circuit further comprises:

a fifth transistor coupled between said first output terminal of said at least one transconductance circuit and said first output terminal of said switching circuit;

a sixth transistor coupled between said first output terminal of said at least one transconductance circuit and said second output terminal of said switching circuit;

a seventh transistor coupled between said second output terminal of said at least one transconductance circuit and said first output terminal of said switching circuit; and

an eighth transistor coupled between said second output terminal of said at least one transconductance circuit and said second output terminal of said switching circuit;

wherein the bases of said fifth transistor and said eighth transistor are coupled together and the bases of said sixth transistor and said seventh transistor are coupled together.

7. The apparatus of Claim 6, further comprising a select circuit having a first terminal coupled to said bases of said first transistor and said fourth transistor, a second terminal coupled to said bases of said second transistor and said third transistor, a third terminal coupled to said bases of said fifth transistor and said eighth transistor, and a fourth terminal coupled to said bases of said sixth transistor and said seventh transistor, wherein said select signal produces complementary signal on said first terminal and said second terminal and produces complementary signals on said third terminal and said fourth terminal.

8. The apparatus of Claim 6, wherein said switching stage further comprises:

a ninth transistor coupled between said first output terminal of said at least one transconductance circuit and a voltage source;

a tenth transistor coupled between said second output terminal of said at least one transconductance circuit and a voltage source;

an eleventh transistor coupled between said third output terminal of said at least one transconductance circuit and a voltage source; and

a twelfth transistor coupled between said fourth output terminal of said at least one transconductance circuit and a voltage source.

9. The apparatus of Claim 1, wherein said first reference voltage and said second reference voltage are programmable voltages.

10. A method of testing a circuit, the method comprising:

providing a first test voltage from a first channel from said circuit and a second test voltage from a second channel from said circuit;

providing a first reference voltage and a second reference voltage;

converting said first test voltage to a first test signal and said second test voltage to a second test signal;

converting said first reference voltage to a first reference signal and said second reference voltage to a second reference signal;

switchably combining said first test signal with one of said second reference signal and said second test signal to form a first combined signal;

switchably combining said first reference signal with one of said second test signal and said second reference signal to form a second combined signal; and

comparing said first combined signal with said second combined signal.

11. The method of Claim 10, wherein said first test signal is a first test current and said second test signal is a second test current and wherein said first reference signal is a first reference current and said second reference signal is a second reference current.

12. The method of Claim 10, wherein said first test signal, said second test signal, said first reference signal, and said second reference signal are voltage signals.

13. The method according to Claim 11, wherein said first combined current is formed by combining said first test current with said second reference current and said second combined current is formed by combining said first reference current with said second test current to realize a differential swing comparison mode.

14. The method according to Claim 11, wherein said first combined current is formed by combining said first test current with said second test current and said second combined current is formed by combining said first reference current with said second reference current to realize a common-mode comparison mode.

15. The method according to Claim 11, further comprising disabling the contribution of said second test current and said second reference current wherein said first combined current comprises said first test current and said second combined current comprises said first reference current to realize a P-channel comparison mode.

16. The method according to Claim 11, further comprising disabling the contribution of said first test current and said first reference current wherein said first combined current comprises one of said second test current and said second reference current and said second current comprises one of said second test current and said second reference current to realize an N-channel comparison mode.

17. A method of testing a circuit, the method comprising:

providing a first test voltage from a first channel from said circuit and a second test voltage from a second channel from said circuit;

providing a first reference voltage and a second reference voltage;

converting said first test voltage to a first test current and said second test voltage to a second test current;

converting said first reference voltage to a first reference current and said second reference voltage to a second reference current;

switchably combining said first test current with one of said second reference current and said second test current to form a first combined current;

switchably combining said first reference current with one of said second test current and said second reference current to form a second combined current; and

comparing said first combined current with said second combined current.